

incrementing a column address from the starting column address when the LSB is a logic "0"; and

decrementing a column address from the starting column address when the LSB is a logic "1".

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33. The method of claim 31 wherein the act of controlling the count direction of the bust counter responsive to the NLSB in the interleave operating mode comprises:

incrementing a column address from the starting column address when the NLSB is a logic "0"; and

decrementing a column address from the starting column address when the NLSB is a logic "1".

REMARKS

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with Markings to Show Changes Made".

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

31 [32]. A method of controlling a bust counter for a memory device operable in a 2-bit prefetch mode, the method comprising:

in a serial operating mode, controlling the count direction of the bust counter responsive to the state of the least significant bit (“LSB”) of a starting column address; and

in an interleave operating mode, controlling the count direction of the bust counter responsive to the state of the next to least significant bit (“NLSB”) of the starting column address.

32 [33]. The method of claim 31[32] wherein the act of controlling the count direction of the bust counter responsive to the LSB in the serial operating mode comprises:

incrementing a column address from the starting column address when the LSB is a logic “0”; and

decrementing a column address from the starting column address when the LSB is a logic “1”.

33 [34]. The method of claim 31[32] wherein the act of controlling the count direction of the bust counter responsive to the NLSB in the interleave operating mode comprises:

incrementing a column address from the starting column address when the NLSB is a logic “0”; and

decrementing a column address from the starting column address when the NLSB is a logic “1”.